M.Sc. (Electronics) (NEP Pattern) Semester-I

NEP-32 / PSCELT102 - Paper-II : Analog and Digital System

P. Pages : 2 **GUG/S/25/15088**

Time : Three Hours * 2 7 3 2 * Max. Marks : 80

Notes : 1. All questions are compulsory and carry equal marks.
2. Draw neat and label diagrams wherever necessary.

Either :

1. a) Design a differential amplifier using field effect transistor. **8**

b) What is a current Mirror? How it is used in impedance matching? **8**

OR

c) Explain analysis of BJT for multistage amplifiers? **8**

d) Explain the Common Source amplifier with active Loads? **8**

Either :

2. a) Explain Operational Amplifiers (OPAMP) as a differentiator and derive the expressions for its output voltage. **8**

b) Explain Schmitt trigger circuit. **8**

OR

c) Explain the voltage-to-current converter circuit using Op-amp. What are its applications? **8**

d) What is Phase locked loop (PLL)? Draw and explain its use as a frequency synthesizer. **8**

Either :

3. a) Explain 4x4 keyboard encoder. **8**

b) Explain Sequential circuits? Draw state diagrams, characteristic equation of D-flip-flops. **8**

OR

c) Explain the difference between synchronous and asynchronous counters. Design a 3 bit ripple counter using TFFS. **8**

d) Describe of counters with lockout prevention. **8**

Either :

4. a) Explain the design of a sequence detector circuit. **8**

b) Explain the steps involved in design of ALU in digital circuits using logic gates. **8**

OR

c) What is a PLA? Show how PLA can be programmed to implement the sum and carry outputs of a full adder? **8**

d) What is CPLD? How is it different from FPGA? State advantage of using CPLDs. **8**

5. Solve the followings:

a) Explain small signal circuit analysis. **4**

b) What is active filter? Explain. **4**

c) State difference between combinational and sequential circuits. **4**

d) Write a note on ring counter. **4**

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